REMARKS

Claims 1-22 are pending. Claims 1, 2, 9, 13, 14, and 21 have been amended.

Claims 1-8 and 13-20 stand rejected under 35 U.S.C. § 103(a) for obviousness over a combination of newly cited U.S. Patent No. 6,002,273 to Humphreys ("Humphreys") and previously cited U.S. Patent No. 6,049,233 to Shurboff ("Shurboff). The remaining claims 9-12, 21, and 22 stand rejected for obviousness over a combination of Humphreys and Shurboff and previously cited IBM Technical Disclosure Bulletin XP-002104823 by Turner ("Turner").

These rejections should be reconsidered and withdrawn in view of the current amendments to all of the independent and some of the dependent claims. Neither the combination of Humphreys and Shurboff nor the combination of Humphreys, Shurboff, and Turner teaches or even suggests all of the features recited in the claims as amended, and thus Humphreys, Shurboff, and Turner are insufficient as bases for a *prima facie* case of obviousness.

The claims as amended relate to sigma-delta modulators that generate divisional values for fractional-N dividers in phase-locked loops. In such devices and methods, out-of-band modulator noise may be folded back into the loop bandwidth by rectification due to different negative and positive slopes of the phase detector, thus resulting in inferior noise performance compared to their integer-divide counterparts, such as those described in Turner. Applicants solve this problem in part by shifting the operating point away from the origin of the transfer function; the phase detector operates in a linear region even for positive and negative phase differences.

As recited in claim 1, as amended, for example, the operating point is also shifted "so that a nonzero output signal corresponds to a nonzero phase difference between the first and second signals, and the nonzero phase difference is close to or larger than an amount of time equal to at least a number of cycles of the phase-locked loop output signal." Furthermore, as recited in claim 2, as amended, for example, "the amount of time is such that delta-sigma ($\Delta\Sigma$) noise is confined to one side of a zero-crossing of the phase detector output signal."

It is again respectfully submitted that shifting the operating point is not found in Humphreys, Shurboff, or Turner, let alone shifting according to a nonzero phase difference that is close to or larger than a particular amount of time, as in claim 1, or shifting such that noise is confined to one side of the zero crossing of the phase detector's output signal. These features are described in the application at page 12, lines 5-13, for example, and have been generally discussed in responses to previous Actions.

The pending Action asserts in the paragraph bridging pages 4 and 5 that Shurboff "discloses the nonzero phase difference of the operating point is close to or larger than an amount of time equal to a number of cycles of the second signal", citing Shurboff at col. 1, ll. 10-40, and col. 2, ll. 13-53. After repeated close readings of the cited passages, no such disclosure has been found. The Examiner is respectfully requested to point out with more specificity where in the seven paragraphs cited there is a disclosure of the feature claimed. Moreover, the cited passages also simply do not teach or suggest the claimed nonzero phase difference that is close to or larger than an amount of time equal to at least a number of cycles of the phase-locked loop output signal or the claimed amount of time is such that delta-sigma ($\Delta\Sigma$) noise is confined to one side of a zero-crossing of the phase detector output signal.

The relevant parts of the cited passages of Shurboff simply state the problem, "To optimize the phase noise of the fractional-n synthesizer, equal amounts of charge must be added and subtracted from the loop for a given phase offset" between the reference and feedback signals, and then state Shurboff's solution, "Equalizing the charges is accomplished by adding in unequal delay circuits in the reset path of the phase detector." Shurboff, col. 1, ll. 36-39; col. 2, ll. 51-53. The cited passages say nothing about what those "unequal delay circuits" should be, and they also say nothing about anything other than equalizing the charges, e.g., they do not suggest shifting an operating point.

The most that Shurboff says about the delay circuits may be at col. 3, ll. 1-35, where the second delay circuit 112 delays a pulse "as much as 20 ns", but this says nothing about a nonzero phase difference that is a shifted operating point of the phase

detector. Shurboff discloses that the circuit 112 is not permitted to have zero delay when the circuit 116 has zero delay because it degrades noise performance of the phase detector when the loop is locked. To avoid the degradation, the circuit 112 is adjusted to "realign the up current and the down current" (col. 3, ll. 18-20), which is nothing more than consistent with Shurboff's solution stated in col. 2, ll. 51-53, that charges are equalized by adding unequal delay circuits in the reset path. The same is also disclosed at col. 3, ll. 31-35.

The statement on page 4 of the pending Action that Shurboff's phase detector linearization by adding unequal delay circuits "is equivalent to shifting the operating point of the phase detector" confuses the concepts of a linearized transfer function and an operating point on that transfer function. Shurboff's unequal delay circuits linearize the phase detector's transfer function, but linearization says nothing about where to place the operating point on a linearized transfer function. To the extent that Shurboff speaks to the question of where to place the operating point, Shurboff discloses placing the operating point at the origin, not displaced away from the origin, when it states that "with the loop in lock, . . . the phase detector circuit 500 generates substantially equal up current and down current pulses". Col. 5, ll. 55-58 (underlining added). This was first pointed out in the Amendment filed on October 22, 2003.

Accordingly, Shurboff's idea of equalizing charges with unequal delay circuits is simply not the same as and would not have suggested the claimed feature of an operating point shifted by a nonzero phase difference close to or larger than an amount of time equal to at least a number of cycles of the phase-locked loop output signal, as in the independent claims as amended.

Moreover, Shurboff's idea of equalizing charges with unequal delay circuits is simply not the same as and would not have suggested the claimed feature of an amount of time such that delta-sigma ($\Delta\Sigma$) noise is confined to one side of a zero-crossing of the phase detector output signal, as in claim 2 as amended for example. Other than a few general comments about reducing noise, Shurboff says nothing so specific as confining noise to one side as claimed.

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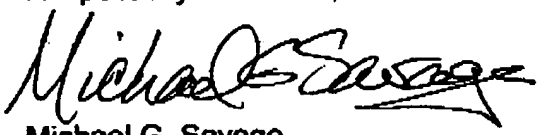
The features described above that are absent from Shurboff are not supplied by either Humphreys or Turner, as admitted in the pending Action. Accordingly, the cited documents fail to support a *prima facie* case of obviousness, which requires, among other things, disclosure of all of the features claimed. In view of these remarks, it is believed unnecessary to discuss in detail the other two requirements of a *prima facie* case, motivation to combine and reasonable expectation of successful combination, except to state that these would also have been lacking from the cited documents.

It is respectively submitted that this application is now in condition for allowance, and an early Notice to this effect is respectfully solicited. If the Examiner has any questions, the undersigned attorney may be telephoned at the number given below. The Examiner may note that a Change of Correspondence Address is filed on the same day as this Amendment.

Respectfully submitted,



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